Amendments to the Specification:

Please replace paragraph [0005] with the following amended paragraph:

[0005] The read/write channels 8 comprise a write channel for recording data and a read channel for reproducing data. A signal-processing technology adopted by the read channel is based on a PRML (Partial Response Maximum Likelihood) technique. It is known that a short error of the order of several bits is generated in a single event in data reproduced by adoption of the PRML technique. In accordance with the conventional technology disclosed in patent reference 1 (Japanese Published Application No. 2000-057709), the 1-event CRCC correction circuit 15 for generating cyclic codes is provided between the read/write channels 8 and the hard disc controller 9 so as to allow a 1-event error (that is, an error generated in a single event) to be corrected. A cyclic code that can be used for correcting an error is called a CRCC (Cyclic Redundancy Check Code) and a technique for correcting an error by using a CRCC is known as a CRCC correction technique. The 1-event CRCC correction circuit 15 carries out a CRCC encoding process and corrects a 1-event error.